MAX9716/MAX9717

Low-Cost, Mono, 1.4W BTL Audio Power Amplifiers

General Description

The MAX9716/MAX9717 audio power amplifiers are ideal for portable audio devices with internal speakers. A bridge-tied load (BTL) architecture minimizes external component count, while providing high-quality audio reproduction. Both devices deliver 1.4W continuous power into a 4Ω load with less than 1% Total Harmonic Distortion (THD) while operating from a single +5V supply. With an 8Ω load, both devices deliver 1W continuous power. These devices also deliver 350mW continuous power into an 8Ω load while operating from a single +3.0V supply. The devices are available as adjustable gain amplifiers (MAX9716/MAX9717A) or with internally fixed gains of 6dB, 9dB, and 12dB (MAX9717B/MAX9717C/MAX9717D), reducing component count.

A low-power shutdown mode disables the bias generator and amplifiers, reducing quiescent current consumption to less than 10nA. These devices feature Maxim's industry-leading, comprehensive click-and-pop suppression that reduces audible clicks and pops during startup and shutdown.

The MAX9717 features a headphone sense input ($\overline{BTL}$/SE) that senses when a headphone is connected to the device, disables the BTL slave driver, muting the speaker while driving the headphone as a single-ended load.

The MAX9716 is pin compatible with the LM4890 and is available in 9-bump UCSP™, 8-pin TDFN (3mm x 3mm), and 8-pin µMAX® packages. The MAX9717 is available in 9-bump UCSP, 8-pin TDFN, and 8-pin µMAX packages. Both devices operate over the -40°C to +85°C extended temperature range.

Applications

Mobile Phones

Portable Devices

PDAs

Features

- **2.7V to 5.5V Single-Supply Operation**
- **1.4W into 4Ω at 1% THD+N**
- **10nA Low-Power Shutdown Mode**
- **73dB PSRR at 1kHz**
- **No Audible Clicks or Pops at Power-Up/Down**
- **Internal Fixed Gain to Reduce Component Count (MAX9717B/C/D)**
- **Adjustable Gain Option (MAX9716/MAX9717A)**
- **$\overline{BTL}$/SE Input Senses when Headphones are Connected (MAX9717)**
- **Pin Compatible with LM4890 (MAX9716)**
- **Pin Compatible with TPA711 (MAX9717A)**
- **Available in Compact, Thermally Enhanced µMAX and TDFN (3mm x 3mm) Packages**

Ordering Information

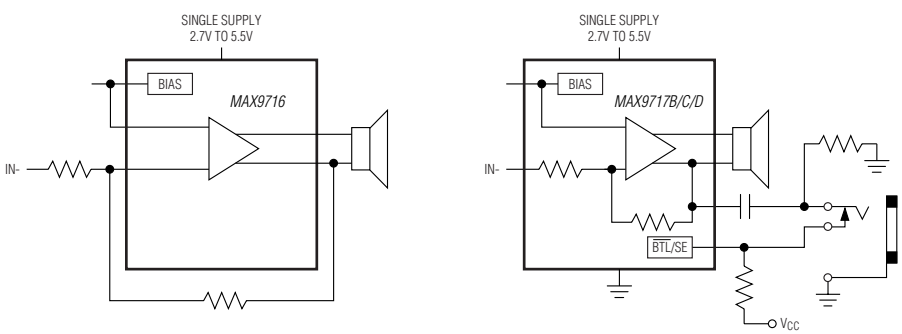
PART	TEMP RANGE	PIN-PACKAGE	GAIN (dB)
MAX9716ETA+T	-40°C to +85°C	8 TDFN-EP*	Adj.
MAX9716EBL+TG45	-40°C to +85°C	3 x 3 UCSP	Adj.
MAX9716EUA	-40°C to +85°C	8 µMAX-EP*	Adj.
MAX9716EUA/V+	-40°C to +85°C	8 µMAX-EP*	Adj.

**EP = Exposed pad.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
G45 indicates protective die coating.
/V denotes automotive qualified part.

Ordering Information continued at end of data sheet.

Pin Configurations and Selector Guide appear at end of data sheet.

Simplified Block Diagrams



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to GND) .....-0.3V to +6V
Any Other Pin to GND .....-0.3V to (V_{CC} + 0.3V)
IN_, BIAS, $\overline{SHDN}$, $\overline{BTL}$/SE Continuous Current.....20mA
OUT_ Short-Circuit Duration to GND or V_{CC} (Note 1)...Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
8-Pin µMAX (derate 10.3mW/°C above +70°C) 825mW
9-Bump UCSP (derate 5.2mW/°C above 70°C).....412mW
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Lead(Pb)-Free Packages.....+260°C
Packages Containing Lead(Pb).....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—5V Supply

(V_{CC} = 5V, V_{GND} = 0V, $\overline{SHDN}$ = V_{CC}, T_A = +25°C. C_{BIAS} = 1µF, R_{IN} = R_F = 20kΩ (MAX9716/MAX9717A), IN+ = BIAS (MAX9716), $\overline{BTL}$/SE = GND (MAX9717_), R_L = ∞ connected between OUT+ and OUT-. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	Inferred by PSRR test		2.7		5.5	V
Quiescent Supply Current	I_{CC}	V_{IN-} = V_{IN+} = V_{BIAS} (Note 3), T_A = -40°C to +85°C			4.3	8	mA
Shutdown Supply Current	I_{SHDN}	$\overline{SHDN}$ = GND			0.01	1	µA
$\overline{SHDN}$ Threshold	V_{IH}			1.2			V
	V_{IL}					0.4	
$\overline{BTL}$/SE Threshold	V_{IH}			0.9 x V_{CC}			V
	V_{IL}					0.7 x V_{CC}	
Common-Mode Bias Voltage	V_{BIAS}	(Note 4)		V_{CC}/2 - 6%	V_{CC}/2	V_{CC}/2 + 6%	V
Output Offset Voltage	V_{OS}	V_{IN-} = V_{OUT+}, V_{IN+} = V_{BIAS} (Note 5)			±7	±15	mV
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 5.5V	DC, V_{BIAS} = 1.5V	60	80		dB
		V_{IN+} = V_{BIAS}, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω (Note 6)	f = 217Hz		61		
			f = 1kHz		73		
Output Power	P_{OUT}	R_L = 8Ω, THD+N = 1%, f_{IN} = 1kHz (Note 7)		0.8	1.1		W
		R_L = 4Ω, THD+N = 1%, f_{IN} = 1kHz (Note 7)			1.4		
		R_L = 16Ω, $\overline{BTL}$/SE = V_{CC} (single-ended mode), THD+N = 1%, f_{IN} = 1kHz			0.155		
Total Harmonic Distortion Plus Noise	THD+N	A_V = 6dB, R_L = 8Ω, f_{IN} = 1kHz, P_{OUT} = 0.5W (Note 8)			0.024		%
Output Noise Density	e_n	f_{IN} = 10kHz			106		nV/√Hz
Signal-to-Noise Ratio	SNR	THD+N = 1%			105		dB

ELECTRICAL CHARACTERISTICS—5V Supply (continued)

(V_{CC} = 5V, V_{GND} = 0V, $\overline{SHDN}$ = V_{CC}, T_A = +25°C. C_{BIAS} = 1µF, R_{IN} = R_F = 20kΩ (MAX9716/MAX9717A), IN+ = BIAS (MAX9716), $\overline{BTL}$/SE = GND (MAX9717_), R_L = ∞ connected between OUT+ and OUT-. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Short-Circuit Current Limit	I_{SC}	(Note 9)		1.1		A
Thermal Shutdown Threshold				+160		°C
Thermal Shutdown Hysteresis				15		°C
Power-Up/Enable from Shutdown Time (Note 10)	t_{PU}			250		ms
		C_{BIAS} = 0.1µF		25		
Shutdown Time	t_{SHDN}			5		µs
Input Resistance	R_{IN}	MAX9717B/C/D	12	20	28	kΩ

ELECTRICAL CHARACTERISTICS—3V Supply

(V_{CC} = 3V, V_{GND} = 0V, $\overline{SHDN}$ = V_{CC}, T_A = +25°C. C_{BIAS} = 1µF, R_{IN} = R_F = 20kΩ (MAX9716/MAX9717A), IN+ = BIAS (MAX9716), $\overline{BTL}$/SE = GND (MAX9717_), R_L = ∞ connected between OUT+ and OUT-. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Supply Current	I_{CC}	V_{IN-} = V_{IN+} = V_{BIAS} (Note 3), T_A = -40°C to +85°C			4	8.0	mA
Shutdown Supply Current	I_{SHDN}	$\overline{SHDN}$ = GND			0.01	1	µA
$\overline{SHDN}$ Threshold	V_{IH}			1.2			V
	V_{IL}					0.4	
$\overline{BTL}$/SE Threshold	V_{IH}			0.9 x V_{CC}			V
	V_{IL}					0.7 x V_{CC}	
Common-Mode Bias Voltage	V_{BIAS}	(Note 4)		V_{CC}/2 - 9%	V_{CC}/2	V_{CC}/2 + 9%	V
Output Offset Voltage	V_{OS}	V_{IN-} = V_{OUT+}, V_{IN+} = V_{BIAS} (Note 5)			±7	±15	mV
Power-Supply Rejection Ratio	PSRR	V_{IN+} = V_{BIAS}, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω (Note 6)	f = 217Hz		61		dB
			f = 1kHz		73		
Output Power	P_{OUT}	R_L = 8Ω, THD+N = 1%, f_{IN} = 1kHz (Note 7)			350		mW
		R_L = 4Ω, THD+N = 1%, f_{IN} = 1kHz (Note 7)			525		
Total Harmonic Distortion Plus Noise	THD+N	A_V = 6dB, R_L = 8Ω, f_{IN} = 1kHz, P_{OUT} = 0.5W, V_{CC} = 3V (Note 8)			0.024		%
Output-Noise Density	e_n	f_{IN} = 10kHz			106		nV/√Hz
Signal-to-Noise Ratio	SNR	THD+N = 1%			100		dB

ELECTRICAL CHARACTERISTICS—3V Supply (continued)

(V_{CC} = 3V, V_{GND} = 0V, $\overline{SHDN}$ = V_{CC}, T_A = +25°C. C_{BIAS} = 1µF, R_{IN} = R_F = 20kΩ (MAX9716/MAX9717A), IN+ = BIAS (MAX9716), $\overline{BTL}$/SE = GND (MAX9717_), R_L = ∞ connected between OUT+ and OUT-. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Short-Circuit Current Limit	I_{SC}	(Note 9)		1.1		A
Thermal Shutdown Threshold				+160		°C
Thermal Shutdown Hysteresis				15		°C
Power-Up/Enable from Shutdown Time (Note 10)	t_{PU}			250		ms
		C_{BIAS} = 0.1µF		25		
Shutdown Time	t_{SHDN}			5		µs
Input Resistance	R_{IN}	MAX9717B/C/D	12	20	28	kΩ

Note 1: Continuous power dissipation must also be observed.

Note 2: All specifications are tested at T_A = +25°C. Specifications over temperature (T_A = T_{MIN} to T_{MAX}) are not production tested, and guaranteed by design.

Note 3: Quiescent power-supply current is specified and tested with no load. Quiescent power-supply current depends on the offset voltage when a practical load is connected to the amplifier.

Note 4: Common-mode bias voltage is the voltage on BIAS and is nominally V_{CC}/2.

Note 5: V_{OS} = V_{OUT+} - V_{OUT-}.

Note 6: The amplifier input IN- is AC-coupled to GND through C_{IN}.

Note 7: Output power is specified by a combination of a functional output current test and characterization analysis.

Note 8: Measurement bandwidth for THD+N is 22Hz to 22kHz.

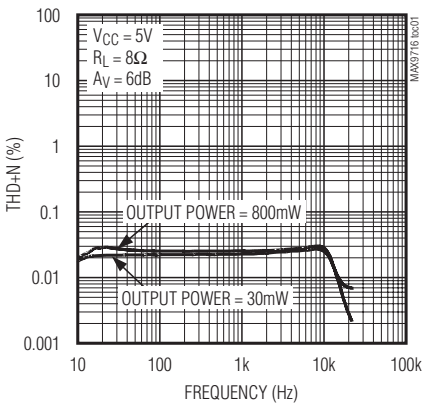
Note 9: Extended short-circuit conditions result in a pulsed output.

Note 10: Time for V_{OUT} to rise to 50% of final DC value.

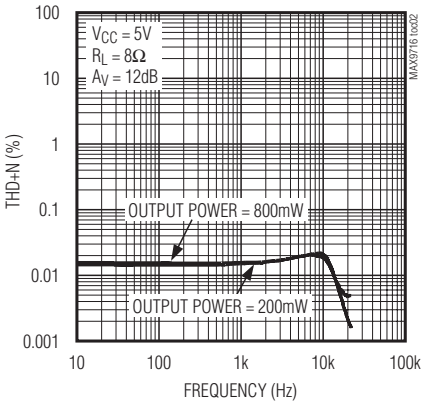
Typical Operating Characteristics

(V_{CC} = 5V, THD+N measurement bandwidth = 22Hz to 22kHz, BTL mode, T_A = +25°C, unless otherwise noted.)

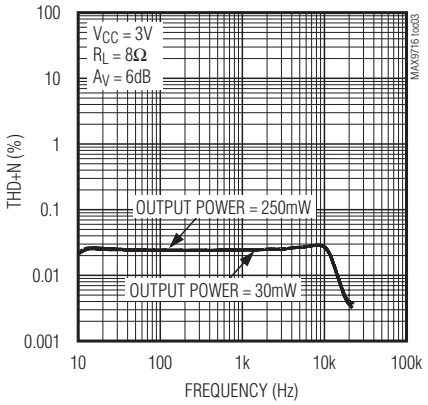
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



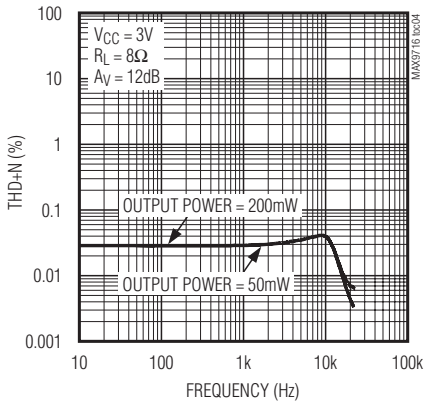
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



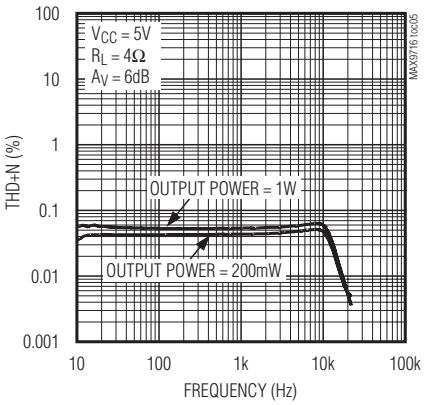
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



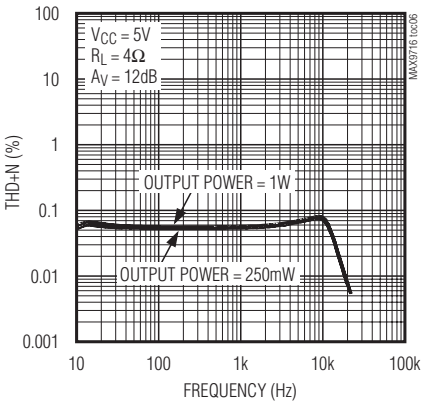
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



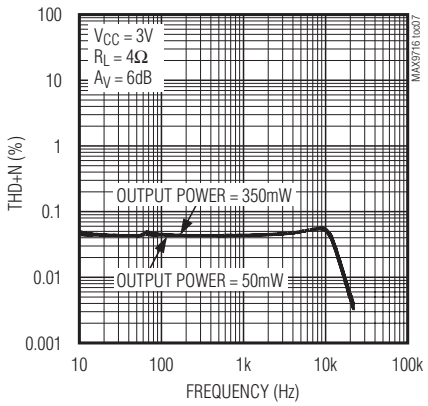
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



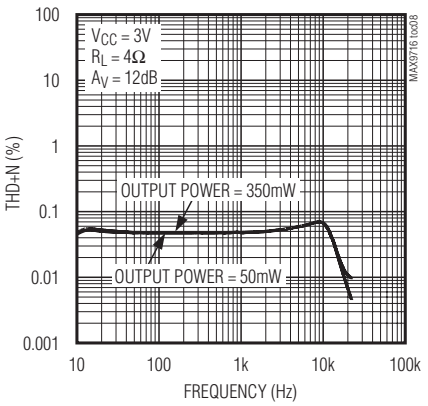
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



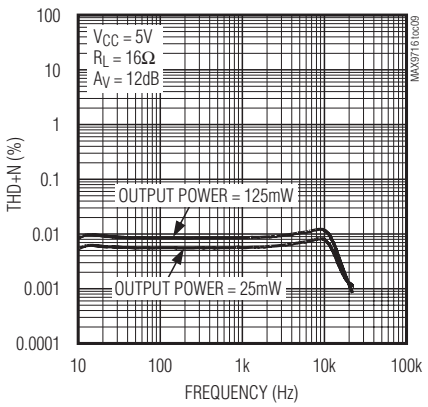
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



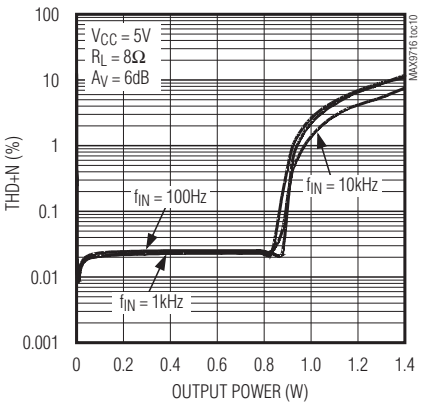
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (SINGLE-ENDED)



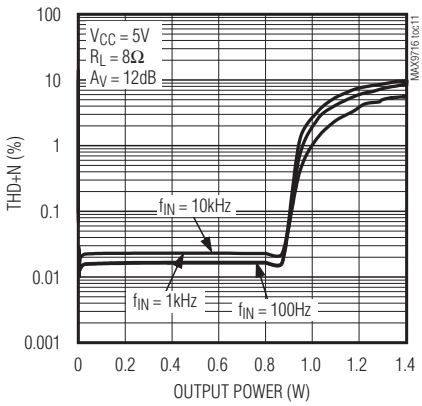
Typical Operating Characteristics (continued)

(V_{CC} = 5V, THD+N measurement bandwidth = 22Hz to 22kHz, BTL mode, T_A = +25°C, unless otherwise noted.)

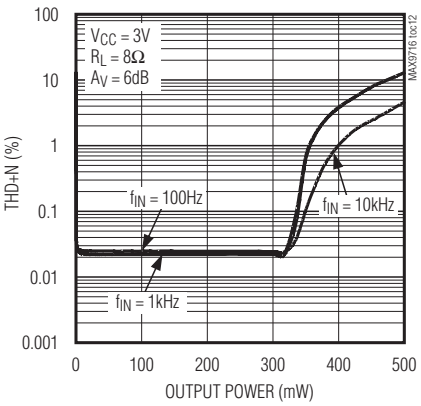
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



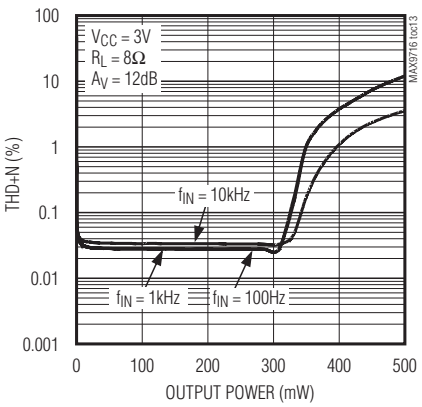
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



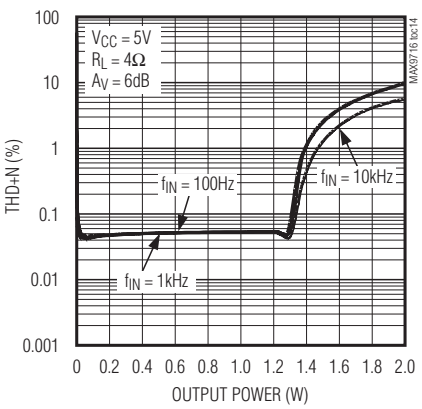
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



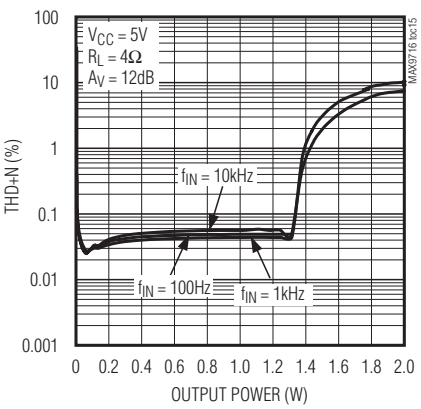
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



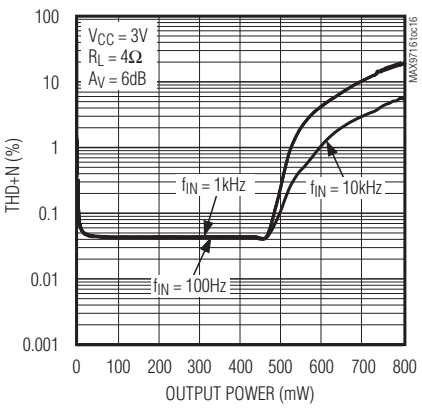
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



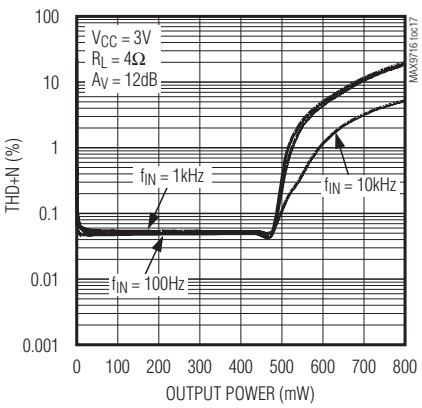
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



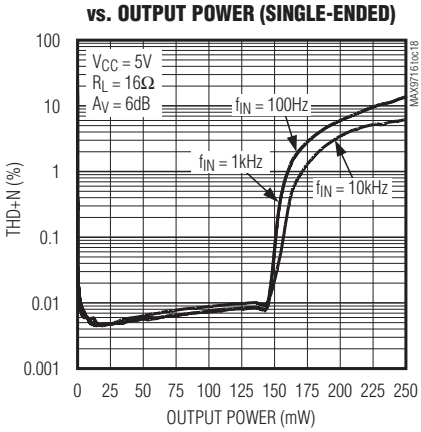
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



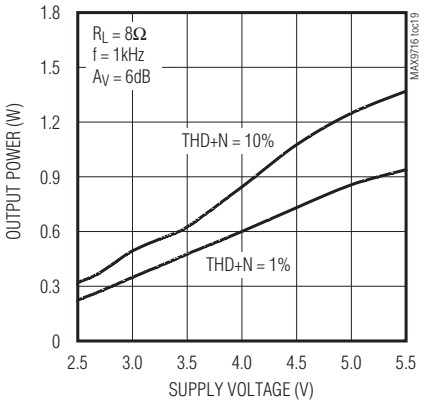
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SINGLE-ENDED)



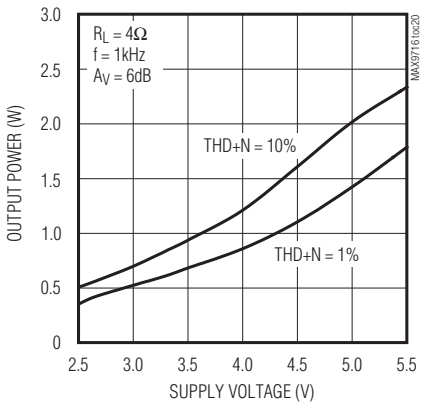
Typical Operating Characteristics (continued)

(V_{CC} = 5V, THD+N measurement bandwidth = 22Hz to 22kHz, BTL mode, T_A = +25°C, unless otherwise noted.)

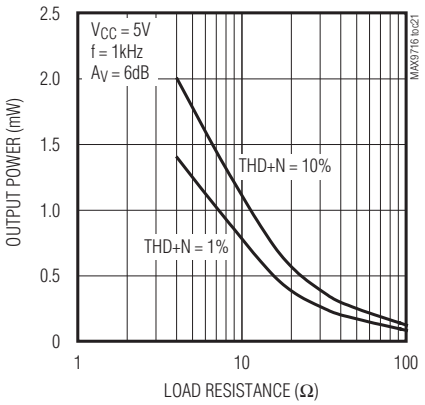
OUTPUT POWER vs. SUPPLY VOLTAGE



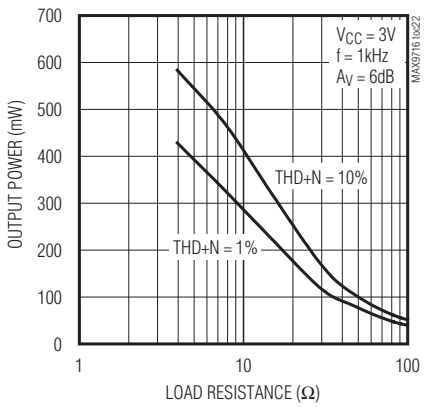
OUTPUT POWER vs. SUPPLY VOLTAGE



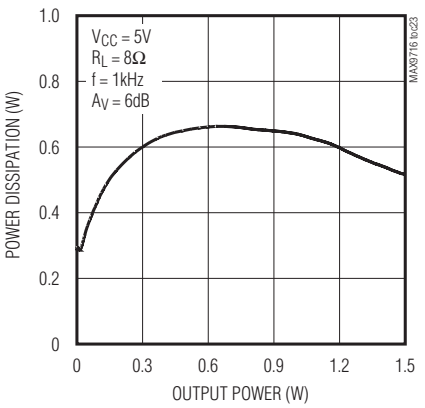
OUTPUT POWER vs. LOAD RESISTANCE



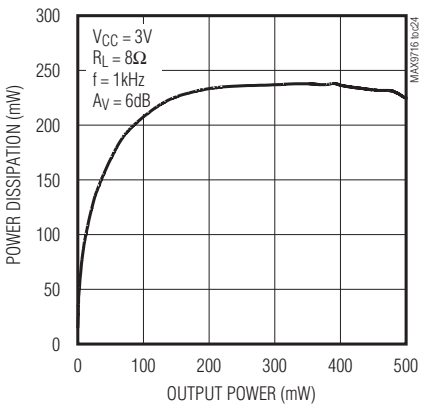
OUTPUT POWER vs. LOAD RESISTANCE



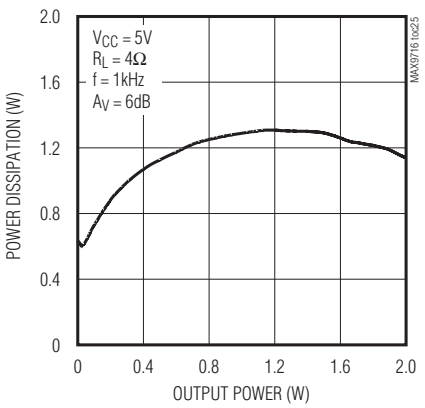
POWER DISSIPATION vs. OUTPUT POWER



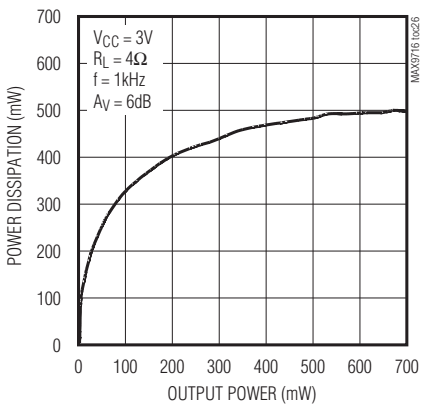
POWER DISSIPATION vs. OUTPUT POWER



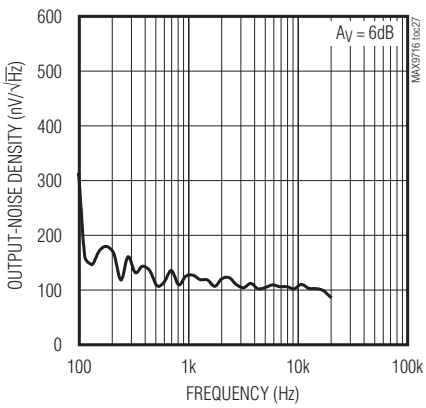
POWER DISSIPATION vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



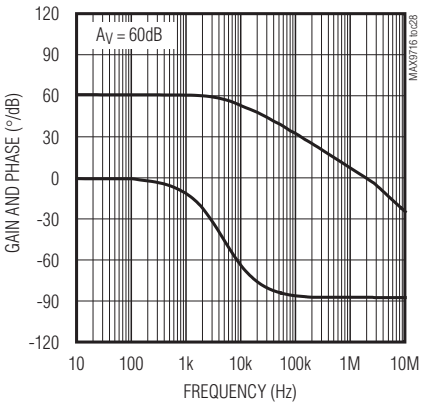
OUTPUT-NOISE DENSITY vs. FREQUENCY



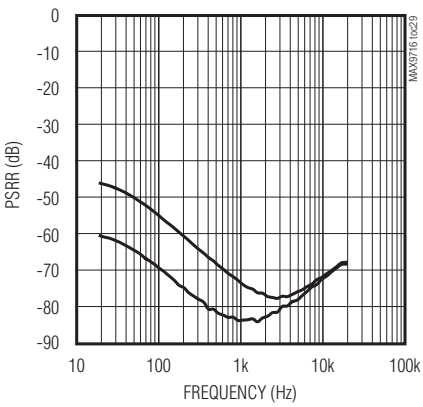
Typical Operating Characteristics (continued)

(V_{CC} = 5V, THD+N measurement bandwidth = 22Hz to 22kHz, BTL mode, T_A = +25°C, unless otherwise noted.)

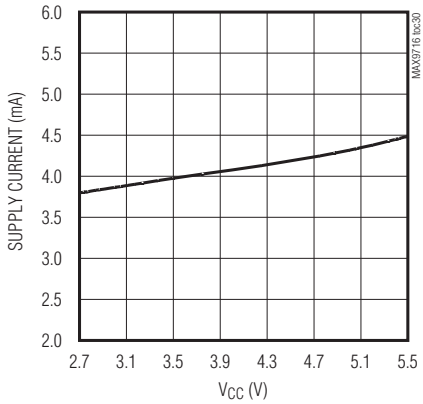
GAIN AND PHASE vs. FREQUENCY



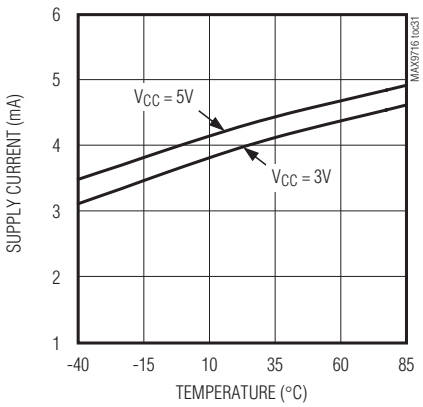
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



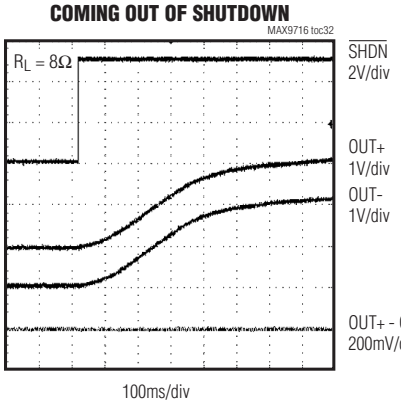
SUPPLY CURRENT vs. V_{CC}



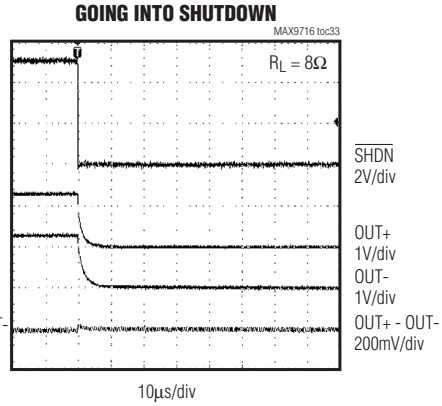
SUPPLY CURRENT vs. TEMPERATURE



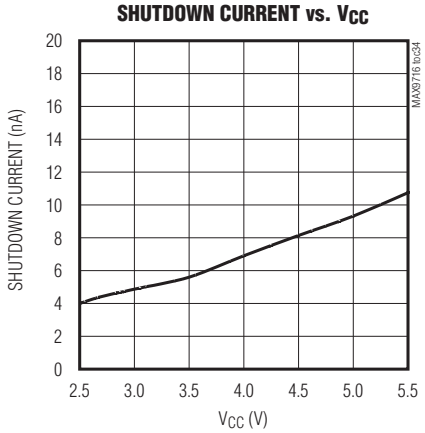
COMING OUT OF SHUTDOWN



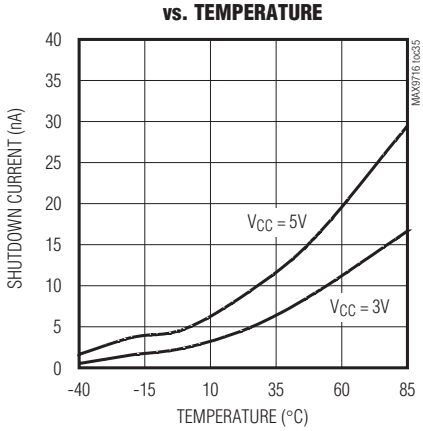
GOING INTO SHUTDOWN



SHUTDOWN CURRENT vs. V_{CC}



SHUTDOWN CURRENT vs. TEMPERATURE



Pin/Bump Description

PIN		BUMP		NAME	FUNCTION
TDFN/µMAX		UCSP			
MAX9716	MAX9717	MAX9716	MAX9717		
1	1	C3	C3	$\overline{SHDN}$	Active-Low Shutdown
2	2	C1	C1	BIAS	DC Bias Bypass Capacitor Connection. Bypass BIAS to ground with a 1µF capacitor.
3	—	A3	—	IN+	Noninverting Input
4	4	A1	A1	IN-	Inverting Input
5	5	A2	A2	OUT+	Bridge Amplifier Positive Output
6	6	B3	B3	V_{CC}	Power Supply. Bypass V_{CC} with a 1µF capacitor to ground.
7	7	B1, B2	B1, B2	GND	Ground
8	8	C2	C2	OUT-	Bridge Amplifier Negative Output. OUT- becomes high-impedance when $\overline{BTL}$/SE is driven high.
—	3	—	A3	$\overline{BTL}$/SE	$\overline{BTL}$/Single-Ended Mode Input. Logic low sets the device in BTL mode. Logic high sets the device in single-ended mode.
—	—	—	—	EP	Exposed Pad (TDFN and µMAX Only). Connect EP to GND.

Detailed Description

The MAX9716/MAX9717 are 1.3W BTL speaker amplifiers. Both devices feature a low-power shutdown mode, and industry-leading click-and-pop suppression. The MAX9717 features a headphone sense input that disables the slave BTL amplifier to drive the headphone as a single-ended load. These devices consist of high output-current audio amps configured as BTL amplifiers (see *Functional Diagrams*). The closed-loop gain of the input op amp sets the single-ended gain of the device. Two external gain resistors set the gain of the MAX9716 and MAX9717A (see the *Gain-Setting Resistor* section). The MAX9717B/C/D feature internally set gains of 6dB, 9dB, and 12dB, respectively.

The output of the first amplifier serves as the input of the second amplifier, which is configured as an inverting unity-gain follower. This results in two outputs, identical in amplitude, but 180° out-of-phase.

BIAS

The MAX9716/MAX9717 operate from a single 2.7V to 5.5V supply and feature an internally generated, common-mode bias voltage of $V_{CC}/2$ referenced to ground. BIAS provides both click-and-pop suppression and sets the DC bias level for the audio outputs. The MAX9716 can be configured as a single-ended or differential input. For single-ended input, connect the noninverting input IN+ to BIAS externally. The MAX9717 BIAS is internally connected to the amplifier noninverting input IN+.

The MAX9717 can only be used with a single-ended input. Always bypass BIAS to ground with a capacitor. Choose the value of the bypass capacitor as described in the *BIAS Capacitor* section. Do not connect external loads to BIAS. Any load lowers the BIAS voltage, affecting the overall performance of the device.

$\overline{BTL}$/SE Control Input

The MAX9717 features a headphone sense input, $\overline{BTL}$/SE, that enables headphone jack sensing to control the power amplifier output configuration. Driving $\overline{BTL}$/SE low enables the slave amplifier (OUT-). Driving $\overline{BTL}$/SE high disables the slave amplifier.

Shutdown Mode

The MAX9716/MAX9717 feature a low-power shutdown mode that reduces quiescent current consumption to 10nA. Entering shutdown disables the bias circuitry, forces the amplifier outputs to GND through an internal 20kΩ resistor. Drive $\overline{SHDN}$ low to enter shutdown mode; drive $\overline{SHDN}$ high for normal operation.

Click-and-Pop Suppression

The MAX9716/MAX9717 feature Maxim's industry-leading click-and-pop suppression circuitry. During startup, the amplifier common-mode bias voltage ramps to the DC bias. When entering shutdown, the amplifier outputs are pulled to GND through an internal 20kΩ resistor. This scheme minimizes the energy present in the audio band.

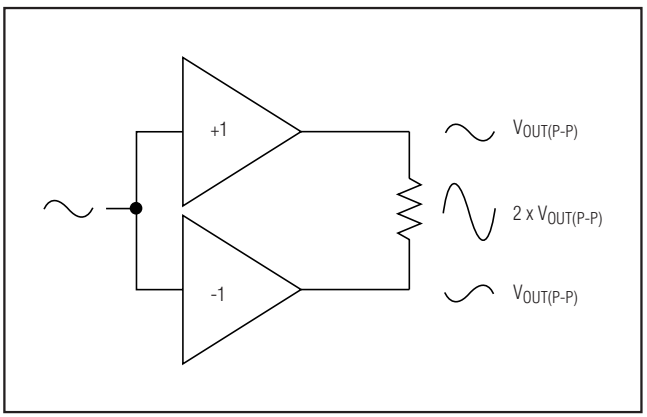


Figure 1. Bridge-Tied Load Configuration

Applications Information

BTL Amplifier

The MAX9716/MAX9717 are designed to drive a load differentially, a configuration referred to as bridge-tied load or BTL. The BTL configuration (Figure 1) offers advantages over the single-ended configuration, where one side of the load is connected to ground. Driving the load differentially doubles the output voltage compared to a single-ended amplifier under similar conditions. Thus, the differential gain of the device is twice the closed-loop gain of the input amplifier. The effective gain is given by:

$$A_V = 2 \times \frac{R_F}{R_{IN}}$$

Substituting 2 x $V_{OUT(P-P)}$ for $V_{OUT(P-P)}$ into the following equations yields four times the output power due to doubling of the output voltage:

$$V_{RMS} = \frac{V_{OUT(P-P)}}{2\sqrt{2}}$$

$$P_{OUT} = \frac{V_{RMS}^2}{R_L}$$

There is no net DC voltage across the load because the differential outputs are each biased at midsupply. This eliminates the need for DC-blocking capacitors required for single-ended amplifiers. These capacitors can be large and expensive, consume board space, and degrade low-frequency performance.

Power Dissipation and Heat Sinking

Under normal operating conditions, the MAX9716/MAX9717 dissipate a significant amount of power. The maximum power dissipation for each package is given in the *Absolute Maximum Ratings* section under Continuous Power Dissipation or can be calculated by the following equation:

$$P_{DISSPKG(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings* section. For example, θ_{JA} of the TDFN package is 41°C/W.

The increase in power delivered by the BTL configuration directly results in an increase in internal power dissipation over the single-ended configuration. The maximum power dissipation for a given V_{CC} and load is given by the following equation:

$$P_{DISS(MAX)} = \frac{2V_{CC}^2}{\pi^2 R_L}$$

If the power dissipation for a given application exceeds the maximum allowed for a given package, reduce power dissipation by increasing the ground plane heat-sinking capability and the size of the traces to the device (see the *Layout and Grounding* section). Other methods for reducing power dissipation are to reduce V_{CC}, increase load impedance, decrease ambient temperature, reduce gain, or reduce input signal.

Thermal-overload protection limits total power dissipation in the MAX9716/MAX9717. Thermal protection circuitry disables the amplifier output stage when the junction temperature exceeds +160°C. The amplifiers are enabled once the junction temperature cools by 15°C. A pulsing output under continuous thermal-overload conditions results as the device heats and cools.

Fixed Gain

The MAX9717B, MAX9717C, and MAX9717D feature internally fixed gains of 6dB, 9dB, and 12dB, respectively (see the *Selector Guide*). Fixed gain simplifies designs, reduces pin count, decreases required footprint size, and eliminates external gain-setting resistors. Resistors R_{IN} and R_F shown in the MAX9717B/C/D *Typical Operating Circuit* are used to achieve each fixed gain.

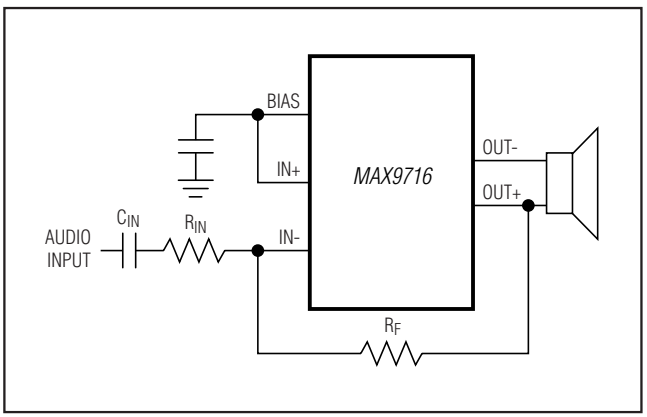


Figure 2. Setting the MAX9716/MAX9717A Gain

Adjustable Gain

Gain-Setting Resistors

External feedback resistors set the gain of the MAX9716 and MAX9717A. Resistors R_F and R_{IN} (see Figure 2*)* set the gain of the amplifier as follows:

$$A_V = 2\left(\frac{R_F}{R_{IN}}\right)$$

Where A_V is the desired voltage gain. Hence, an R_{IN} of 20kΩ and an R_F of 20kΩ yields a gain of 2V/V, or 6dB. R_F can be either fixed or variable, allowing the use of a digitally controlled potentiometer to alter the gain under software control.

The gain of the MAX9717 in a single-ended output configuration is half the gain when configured as BTL output. Choose R_F between 10kΩ and 50kΩ for the MAX9716 and MAX9717A. Gains for the MAX9717B/C/D are set internally.

Input Filter

C_{IN} and R_{IN} form a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimal DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Setting f_{-3dB} too high affects the low-frequency response of the amplifier. Use capacitors with dielectrics that have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, can increase distortion at low frequencies.

Output-Coupling Capacitor

The MAX9717 require output-coupling capacitors to operate in single-ended (headphone) mode. The output-coupling capacitor blocks the DC component of the amplifier output, preventing DC current from flowing to the load. The output capacitor and the load impedance form a highpass filter with a -3dB point determined by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

As with the input capacitor, choose C_{OUT} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response. Load impedance is a concern when choosing C_{OUT}. Load impedance can vary, changing the -3dB point of the output filter. A lower impedance increases the corner frequency, degrading low-frequency response. Select C_{OUT} such that the worst-case load/C_{OUT} combination yields an adequate response. Select capacitors with low ESR to minimize resistive losses and optimize power transfer to the load.

Differential Input

The MAX9716 can be configured for a differential input. The advantage of differential inputs is that any common-mode noise is attenuated and not passed through the amplifier. This input improves noise rejection and provides common-mode rejection (Figure 3). External components should be closely matched for high CMRR. Figure 4 shows the MAX9716 configured for a differential input.

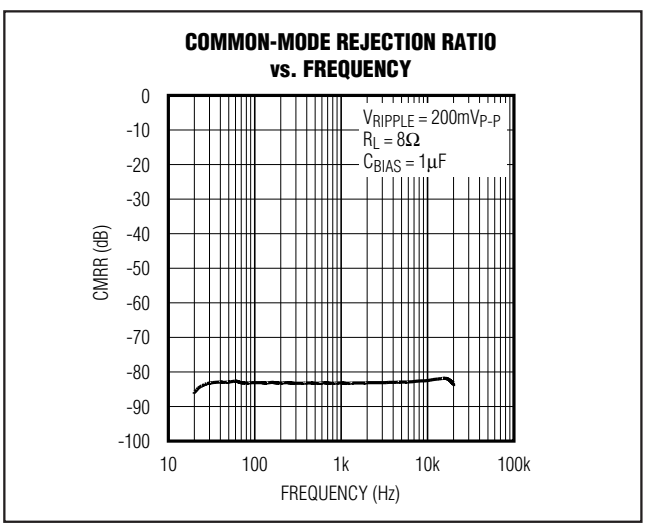


Figure 3. CMRR with Differential Input

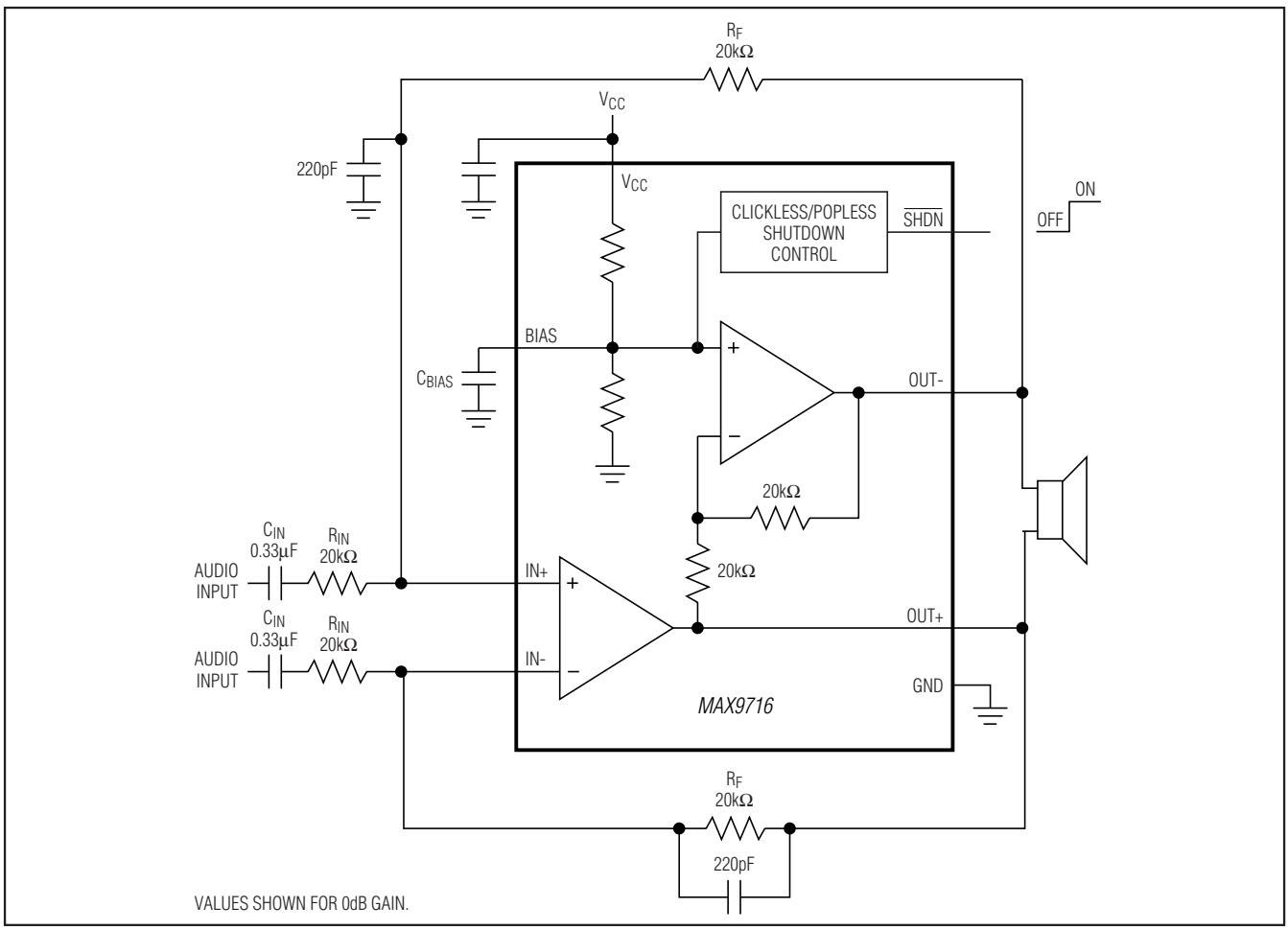


Figure 4. MAX9716 Differential Input

BIAS Capacitor

BIAS is the output of the internally-generated $V_{CC}/2$ bias voltage. The BIAS bypass capacitor, C_{BIAS}, improves the power-supply rejection ratio by reducing power supply and other noise sources at the common-mode bias node. C_{BIAS} also generates the clickless/popless startup DC bias waveform for the speaker amplifiers. Bypass BIAS with a 1µF capacitor to GND. Larger C_{BIAS} values improve PSRR but slow down t_{ON} time. Do not connect external loads to BIAS.

Supply Bypassing

Proper power-supply bypassing ensures low-noise, low-distortion performance. Connect a 1µF ceramic capacitor from V_{CC} to GND. Add additional bulk capacitance as required by the application. Connect the bypass capacitor as close to the device as possible.

Layout and Grounding

Proper PC board layout and grounding is essential for optimizing performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Large traces also aid in moving heat away from the package. Proper grounding improves audio performance and prevents digital switching noise from coupling into the audio signal.

The MAX9716/MAX9717 TDFN and µMAX packages feature exposed thermal pads on their undersides. This pad lowers the thermal resistance of the package by providing a direct-heat conduction path from the die to the printed circuit board. Connect the exposed pad to the ground plane using multiple vias, if required.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the application note, "UCSP—A Wafer-Level Chip-Scale Package" available on Maxim's web site at http://www.maxim-ic.com/ucsp.

UCSP Marking Information

Pin A1 Bump Indicator

AAA: Product ID code

XXX: Lot Code

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	GAIN (dB)
MAX9717AEBL+TG45	-40°C to +85°C	3 x 3 UCSP	Adj.
MAX9717AETA+T	-40°C to +85°C	8 TDFN-EP*	Adj.
MAX9717AEUA	-40°C to +85°C	8 µMAX-EP*	Adj.
MAX9717BEBL+TG45	-40°C to +85°C	3 x 3 UCSP	6
MAX9717BETA+T	-40°C to +85°C	8 TDFN-EP*	6
MAX9717BEUA	-40°C to +85°C	8 µMAX-EP*	6
MAX9717CEBL+TG45	-40°C to +85°C	3 x 3 UCSP	9
MAX9717CETA+T	-40°C to +85°C	8 TDFN-EP*	9
MAX9717CEUA	-40°C to +85°C	8 µMAX-EP*	9
MAX9717DEBL+TG45	-40°C to +85°C	3 x 3 UCSP	12
MAX9717DETA+T	-40°C to +85°C	8 TDFN-EP*	12
MAX9717DEUA	-40°C to +85°C	8 µMAX-EP*	12

**EP = Exposed pad.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
G45 indicates protective die coating.

Selector Guide

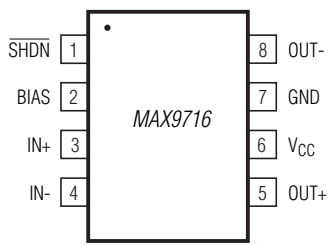
PART	$\overline{BTL}$/SE INPUT	GAIN (dB)
MAX9716	—	Adjustable
MAX9717A	√	Adjustable
MAX9717B	√	6
MAX9717C	√	9
MAX9717D	√	12

Chip Information

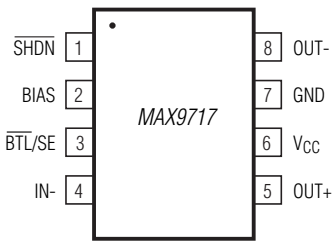
PROCESS: BiCMOS

Pin/Bump Configurations

TOP VIEW

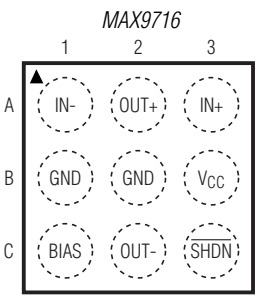


µMAX

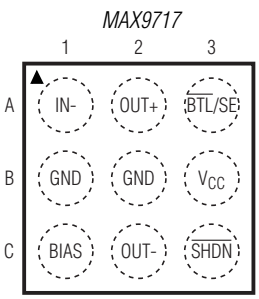


µMAX

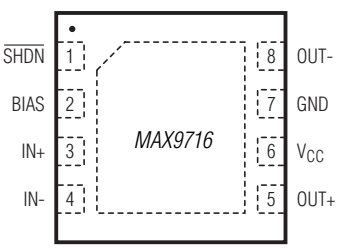
TOP VIEW
(BUMPS ON BOTTOM)



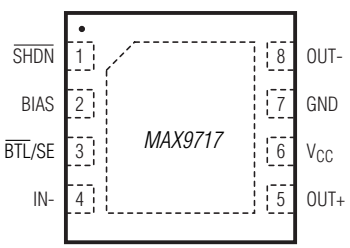
UCSP
(1.5mm x 1.5mm)



UCSP
(1.5mm x 1.5mm)

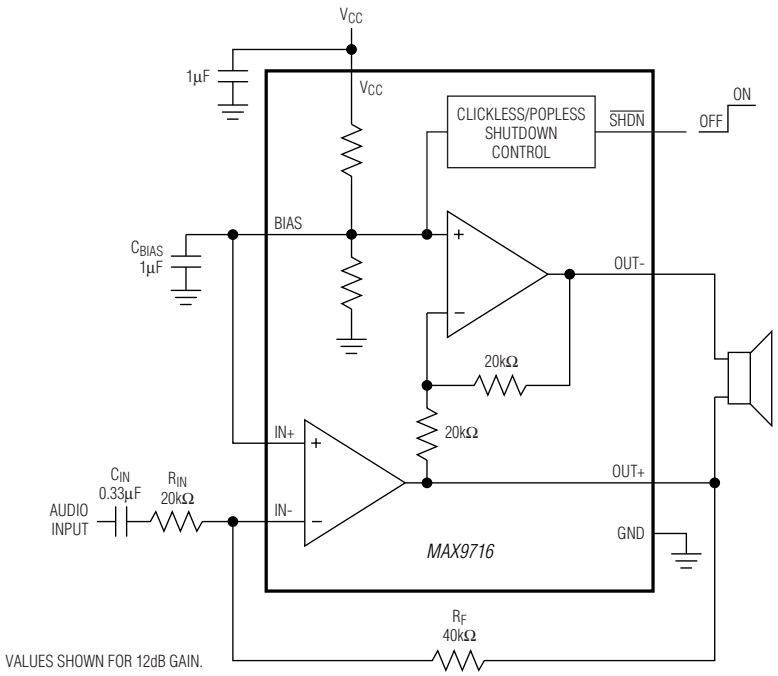


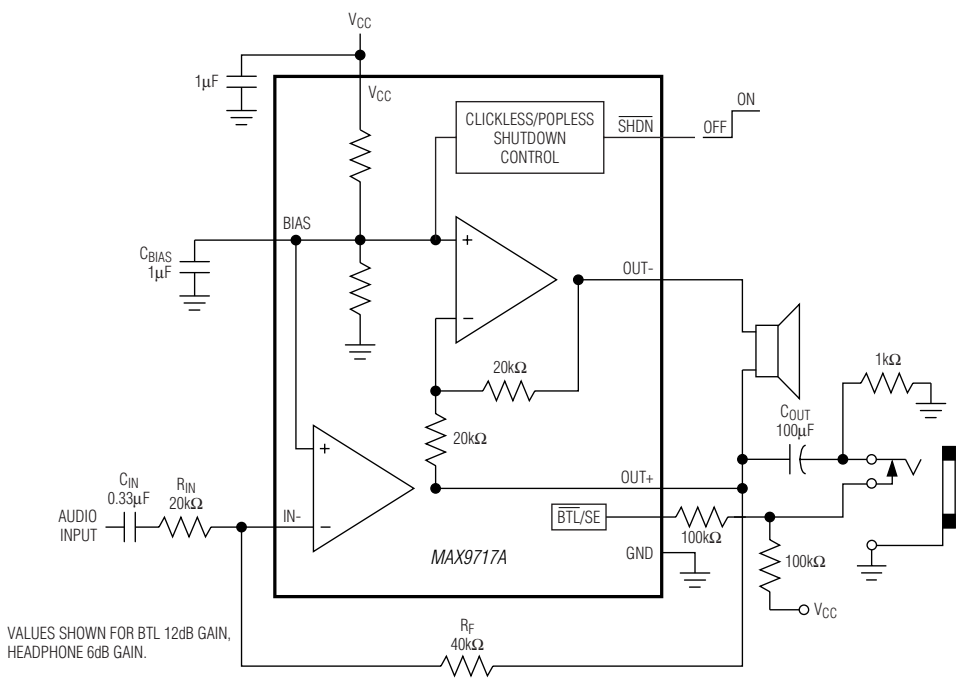
TDFN
(3mm x 3mm x 0.8mm)



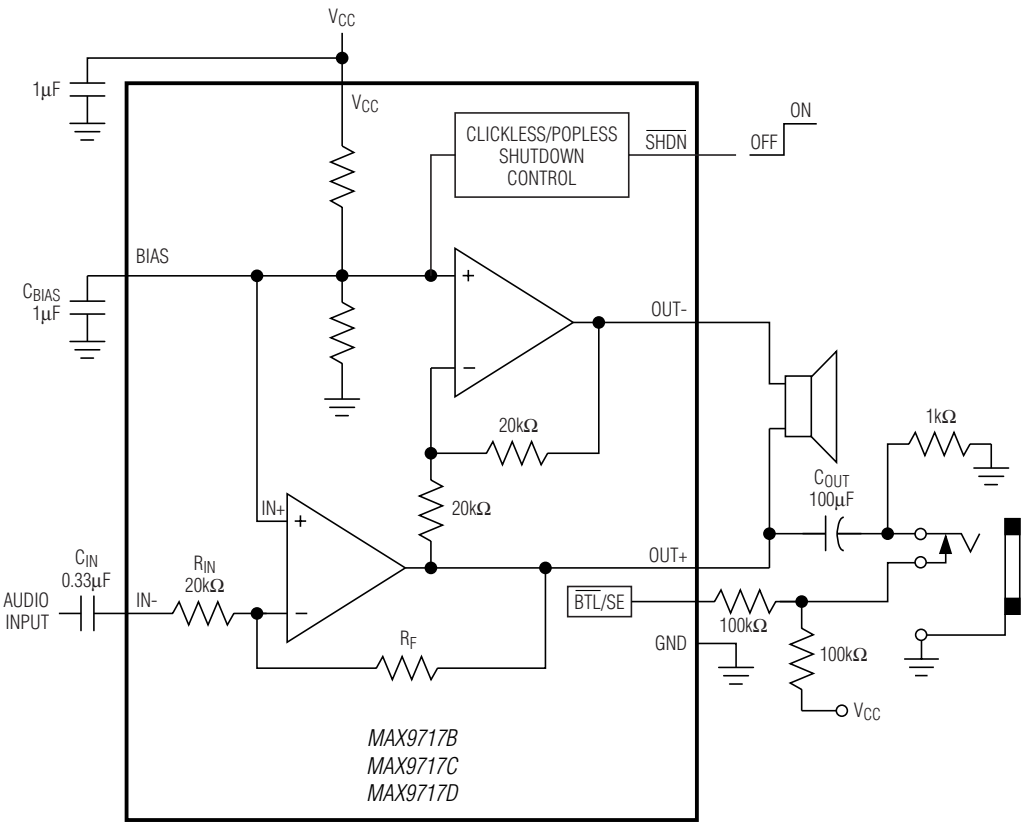
TDFN
(3mm x 3mm x 0.8mm)

Functional Diagrams/Typical Operating Circuits





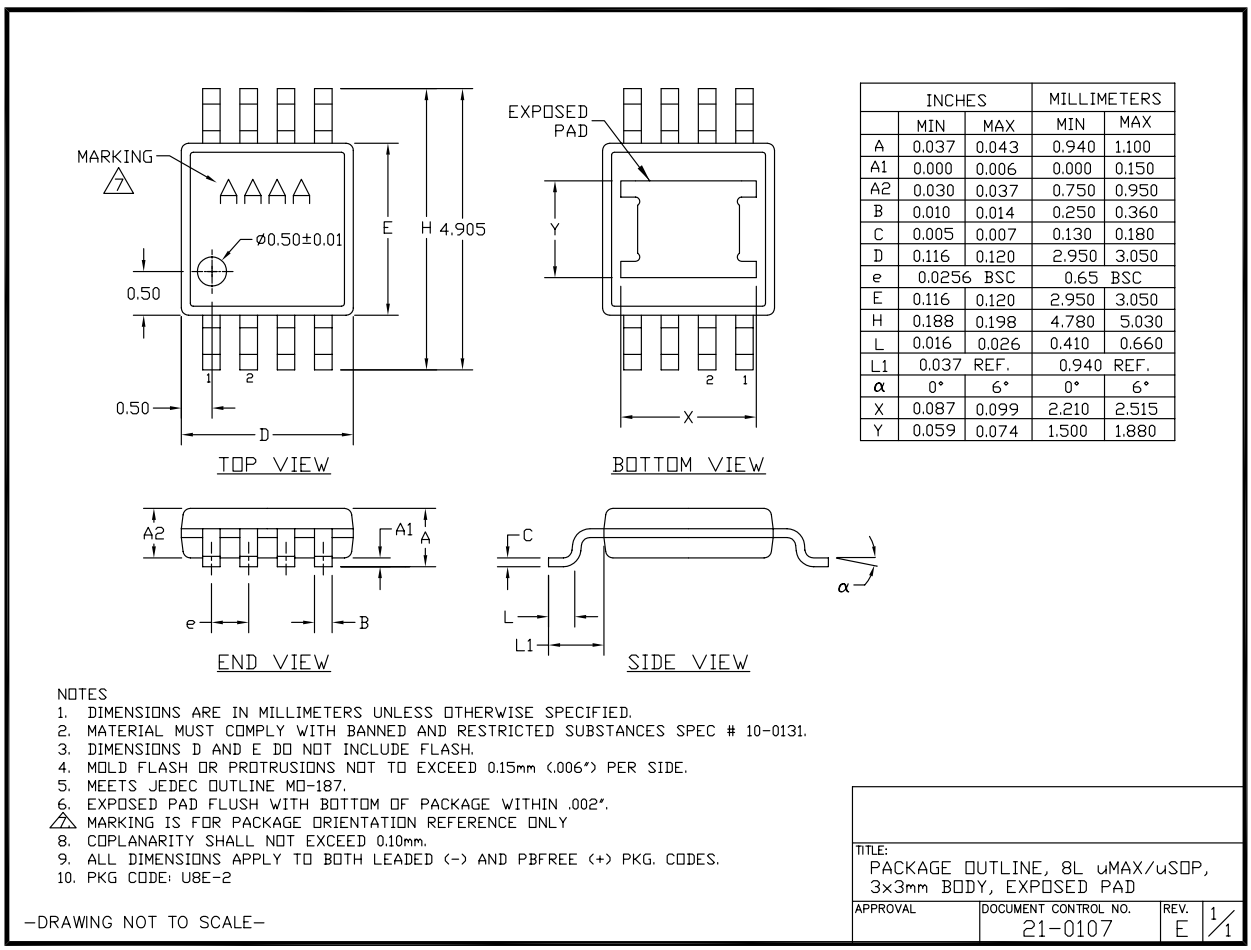
Functional Diagrams/Typical Operating Circuits (continued)



Package Information

For the latest package outline information and land patterns (footprints). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing per-tains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 µMAX	U8E+2	21-0107	90-0145
8 TDFN-EP	T833+1	21-0137	90-0059
9 UCSP	B9+1	21-0093	—



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.037	0.043	0.940	1.100
A1	0.000	0.006	0.000	0.150
A2	0.030	0.037	0.750	0.950
B	0.010	0.014	0.250	0.360
C	0.005	0.007	0.130	0.180
D	0.116	0.120	2.950	3.050
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.950	3.050
H	0.188	0.198	4.780	5.030
L	0.016	0.026	0.410	0.660
L1	0.037 REF.		0.940 REF.	
α	0°	6°	0°	6°
X	0.087	0.099	2.210	2.515
Y	0.059	0.074	1.500	1.880

NOTES
1. DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
3. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
4. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006") PER SIDE.
5. MEETS JEDEC OUTLINE MO-187.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
8. COPLANARITY SHALL NOT EXCEED 0.10mm.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PBFREE (+) PKG. CODES.
10. PKG CODE: U8E-2

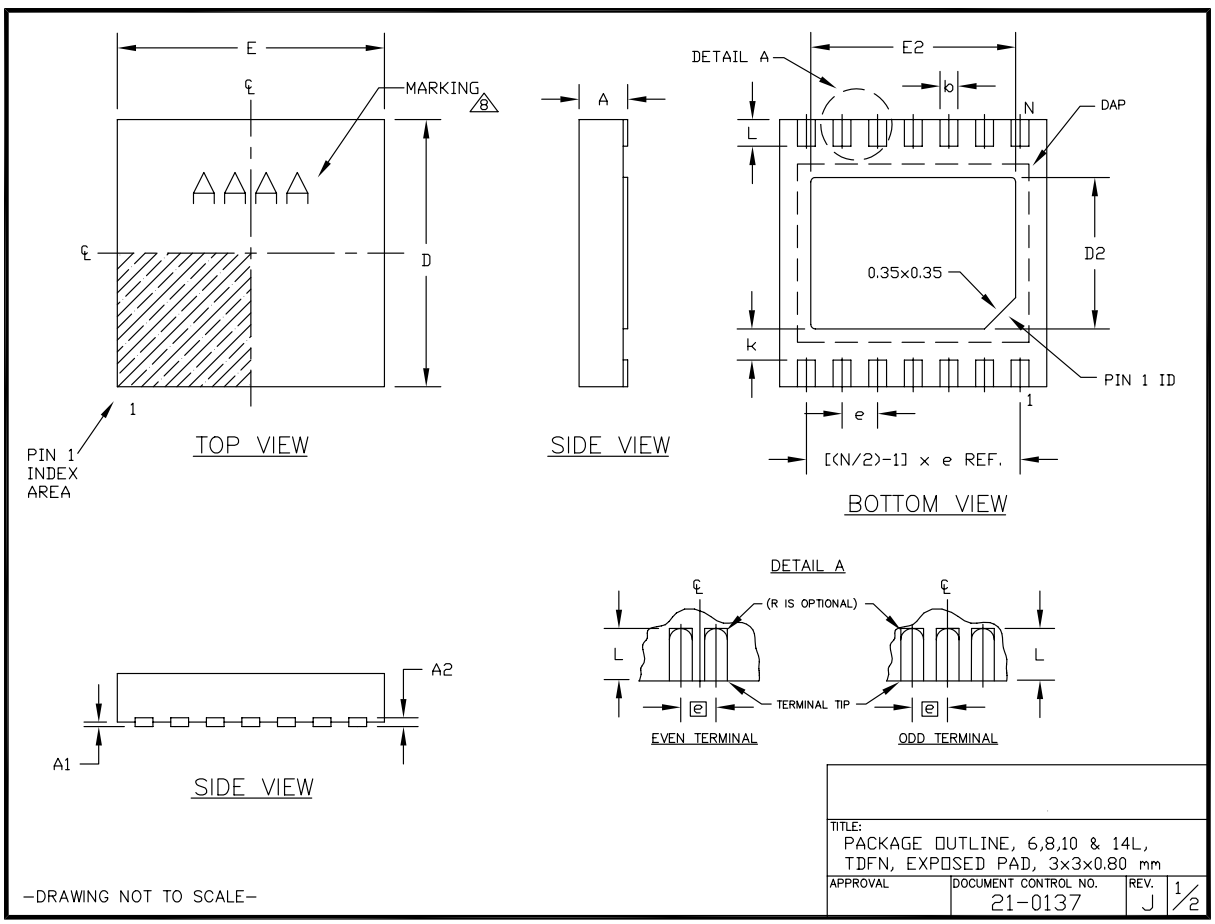
—DRAWING NOT TO SCALE—

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP, 3x3mm BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0107	E	1/1

Package Information (continued)

For the latest package outline information and land patterns (footprints). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing per-tains to the package regardless of RoHS status.



Package Information (continued)

For the latest package outline information and land patterns (footprints). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing per-tains to the package regardless of RoHS status.

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG.CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1]xe
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033MK-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF
T1433-3F	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF

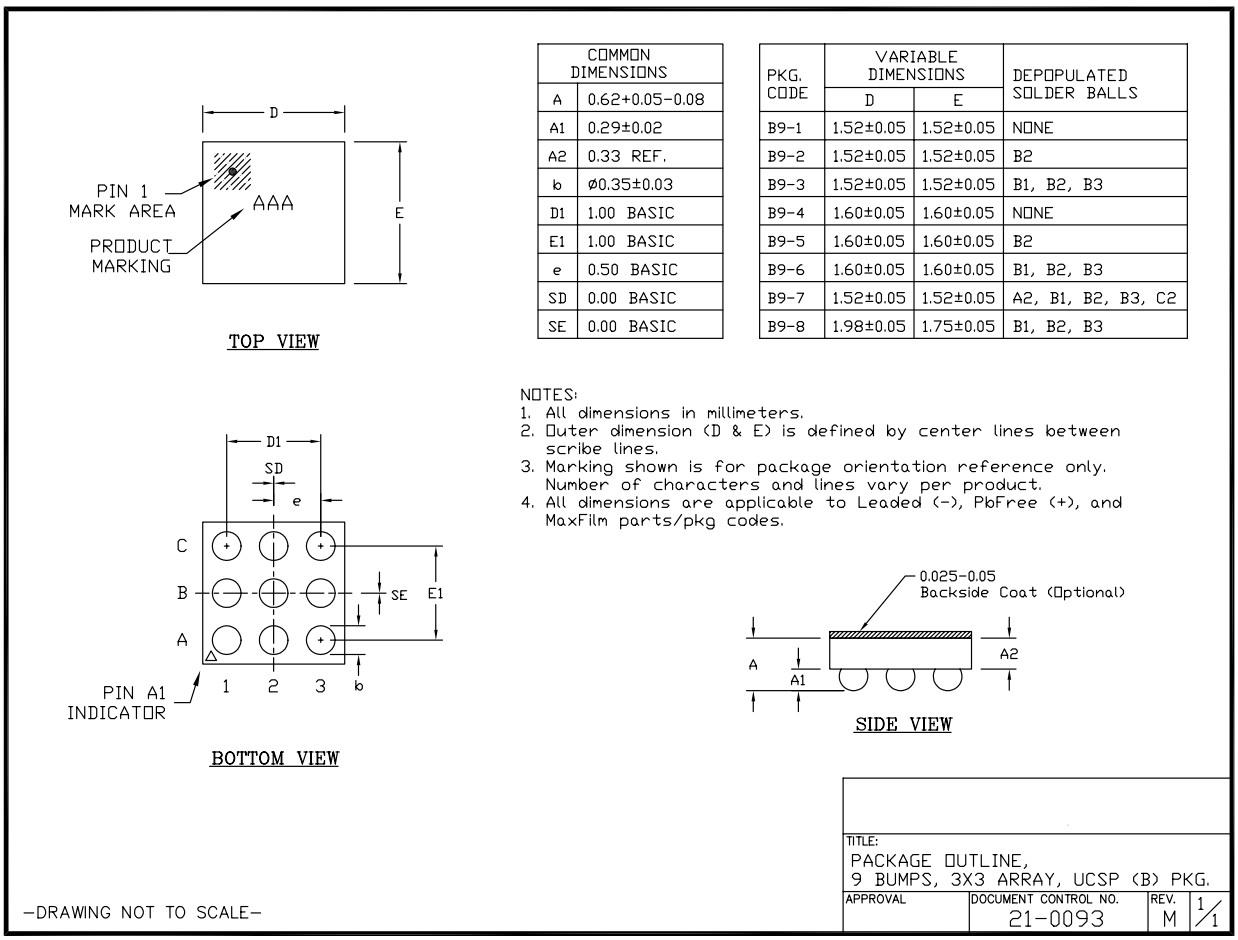
NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0137	REV. J	2/2

Package Information (continued)

For the latest package outline information and land patterns (footprints). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing per-tains to the package regardless of RoHS status.



COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3
B9-7	1.52±0.05	1.52±0.05	A2, B1, B2, B3, C2
B9-8	1.98±0.05	1.75±0.05	B1, B2, B3

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	3/09	Added lead-free and G45 options to *Ordering Information*	1, 13
3	3/12	Add automotive qualified part	1