



CST60P04F P-Ch 40V Fast Switching MOSFETs

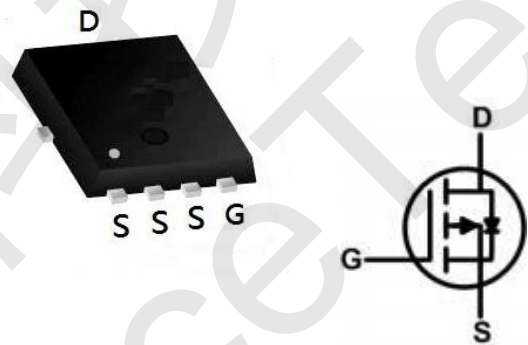
- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

CST60P04F Product Summary



BVDSS	RDSON	ID
-40V	6.4mΩ	-60A

CST60P04F PDFN5060-8L Pin Configuration



CST60P04F Description

The CST60P04F is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The CST60P04F meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

CST60P04F Absolute Maximum Ratings($T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	-60
		$T_C = 100^\circ\text{C}$	-50.6
Pulsed Drain Current ¹	I_{DM}	-320	A
Single Pulse Avalanche Energy ²	EAS	101.25	mJ
Total Power Dissipation	P_D	81.16	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

CST60P04F Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ³	$R_{\theta JA}$	54	$^\circ\text{C}/\text{W}$
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	1.54	$^\circ\text{C}/\text{W}$



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CST60P04F Electrical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static Characteristics							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-40	-	-	V	
Gate-body Leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40V, V_{GS} = 0V$	$T_J = 25^\circ\text{C}$	-	-	-1	pA
			$T_J = 100^\circ\text{C}$	-	-	-100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-1.6	-2.5	V	
Drain-Source on-Resistance ⁴	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -20A$	-	6.4	8.2	m Ω	
		$V_{GS} = -4.5V, I_D = -15A$	-	8.2	11		
Forward Transconductance ⁴	g_{fs}	$V_{DS} = -10V, I_D = -20A$	-	104	-	S	
Dynamic Characteristics⁵							
Input Capacitance	C_{iss}	$V_{DS} = -20V, V_{GS} = 0V, f = 1MHz$	-	5295	-	pF	
Output Capacitance	C_{oss}		-	430	-		
Reverse Transfer Capacitance	C_{rss}		-	385	-		
Gate Resistance	R_g	$f = 1MHz$	-	4.3	-	Q	
Switching Characteristics⁵							
Total Gate Charge	Q_g	$V_{GS} = -10V, V_{DS} = -20V, I_D = -20A$	-	110	-	nC	
Gate-Source Charge	Q_{gs}		-	12.5	-		
Gate-Drain Charge	Q_{gd}		-	23	-		
Turn-on Delay Time	$t_{d(on)}$	$V_{GS} = -10V, V_{DD} = -20V, R_G = 3\Omega, I_D = -20A$	-	16.8	-	ns	
Rise Time	t_r		-	10	-		
Turn-off Delay Time	$t_{d(off)}$		-	65	-		
Fall Time	t_f		-	17	-		
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -20A, di/dt = 100A/\mu s$	-	42	-	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	29	-	nC	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ⁴	V_{SD}	$I_S = -20A, V_{GS} = 0V$	-	-	-1.2	V	
Continuous Source Current	I_S	$T_C = 25^\circ\text{C}$	-	-	-60	A	

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.
2. The EAS data shows Max. rating. The test condition is $V_{DD} = -30V, V_{GS} = -10V, L = 0.1mH, I_{AS} = -45A$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.



CST60P04F Typical Characteristics

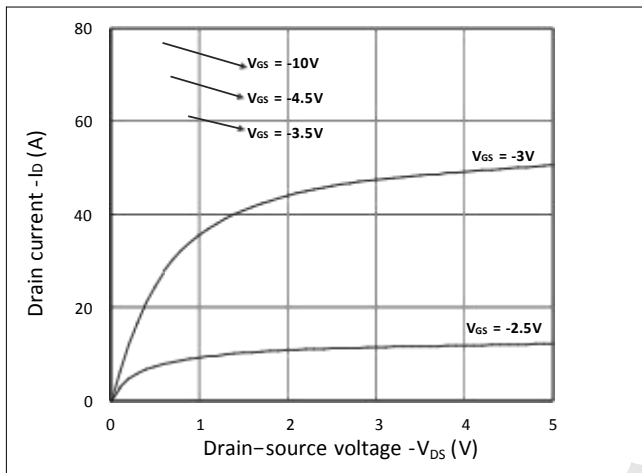


Figure 1. Output Characteristics

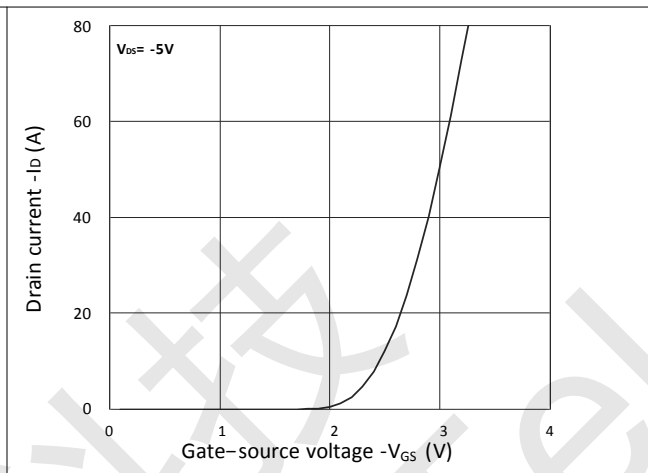


Figure 2. Transfer Characteristics

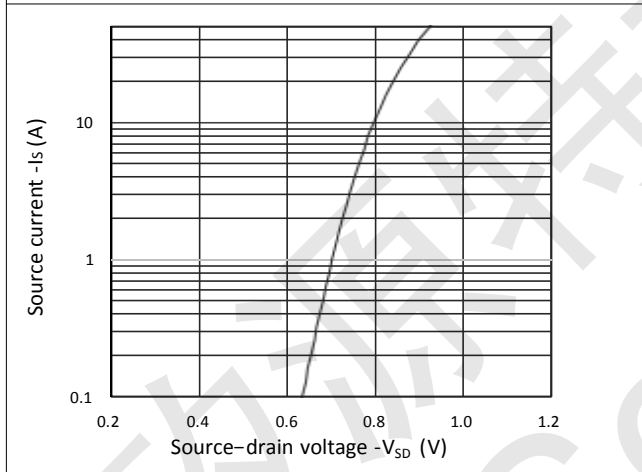


Figure 3. Forward Characteristics of Reverse

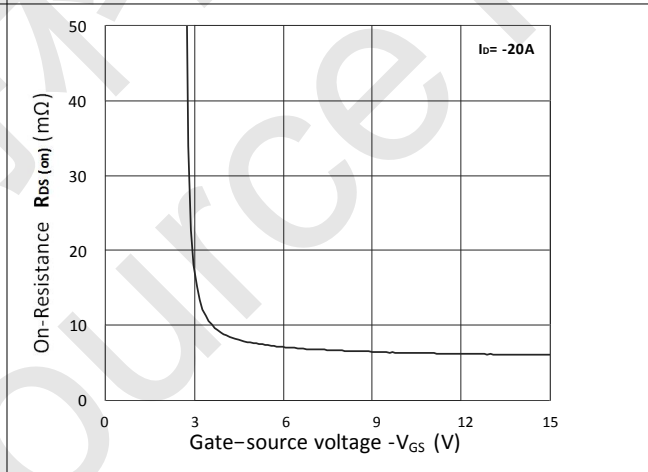


Figure 4. $R_{DS(ON)}$ vs V_{GS}

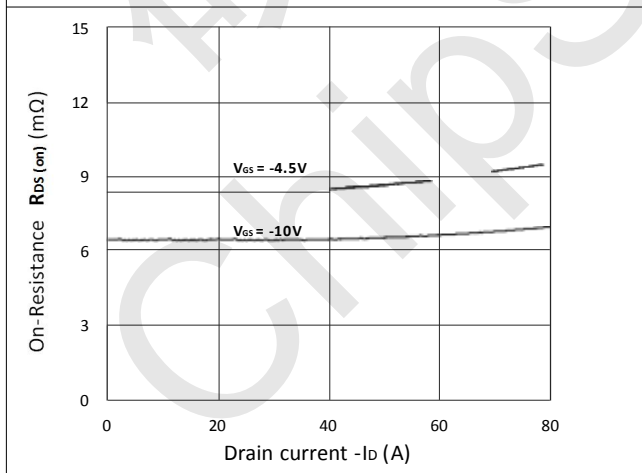


Figure 5. $R_{DS(ON)}$ vs I_D

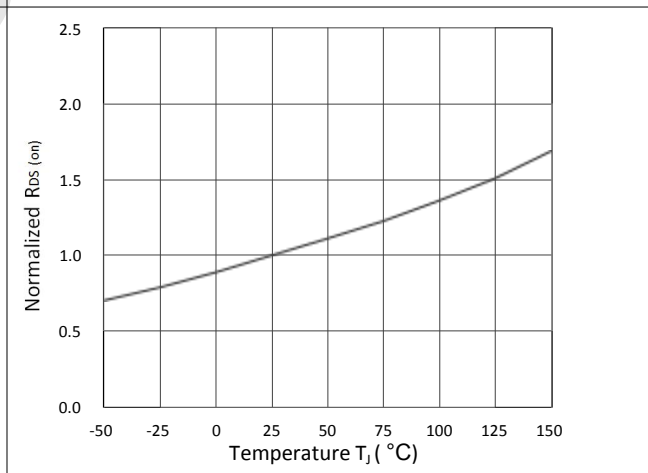


Figure 6. Normalized $R_{DS(ON)}$ vs Temperature

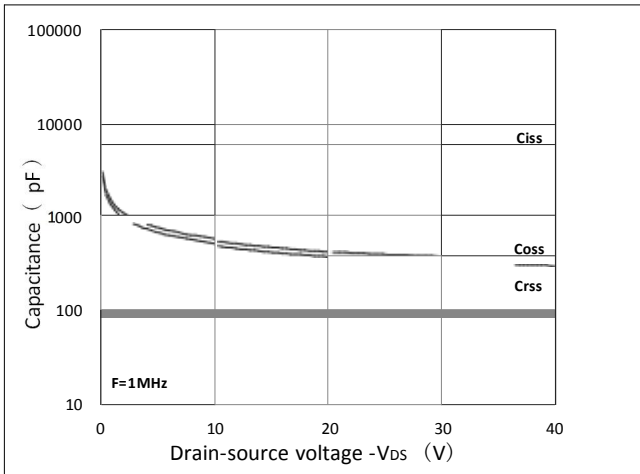


Figure 7. Capacitance Characteristics

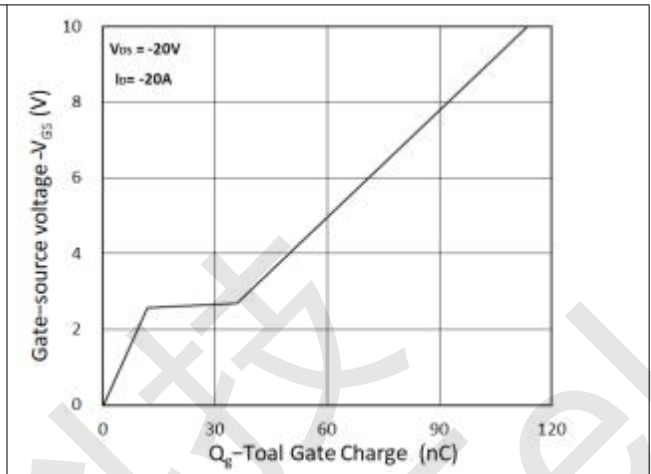


Figure 8. Gate Charge Characteristics

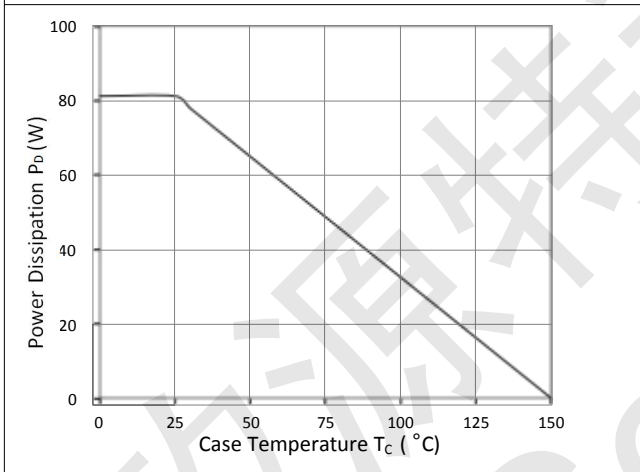


Figure 9. Power Dissipation

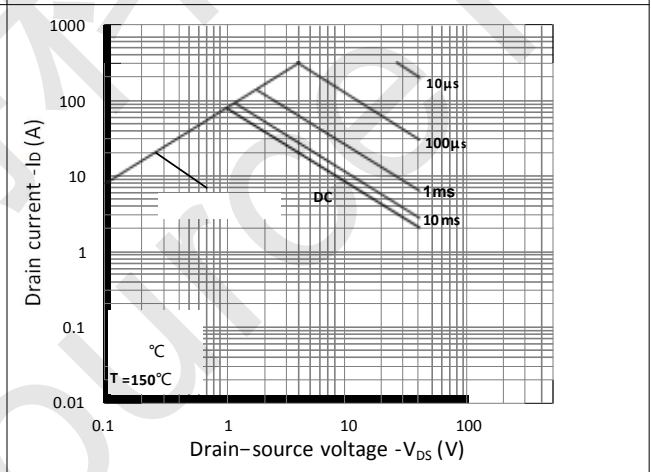


Figure 10. Safe Operating Area

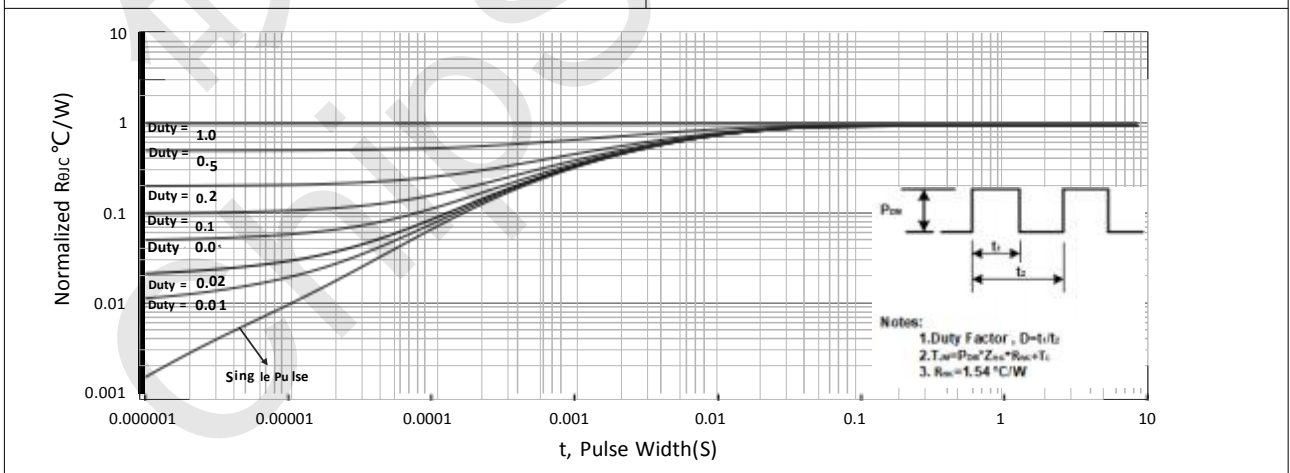
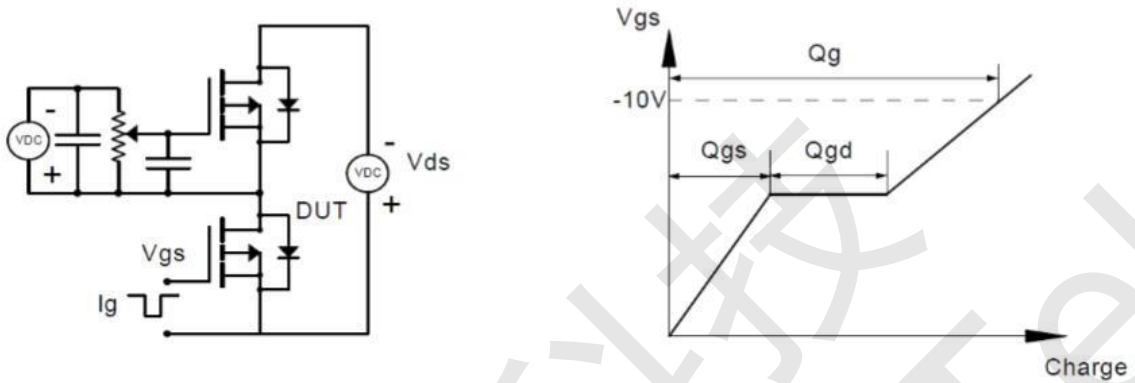


Figure 11. Normalized Maximum Transient Thermal Impedance

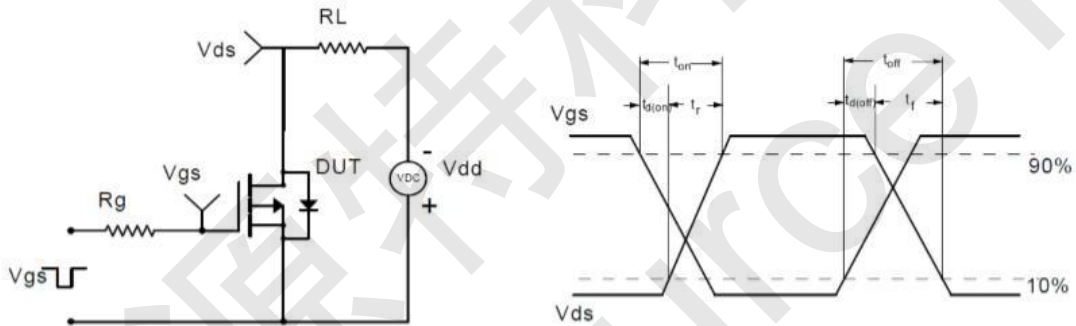


CST60P04F Test Circuit

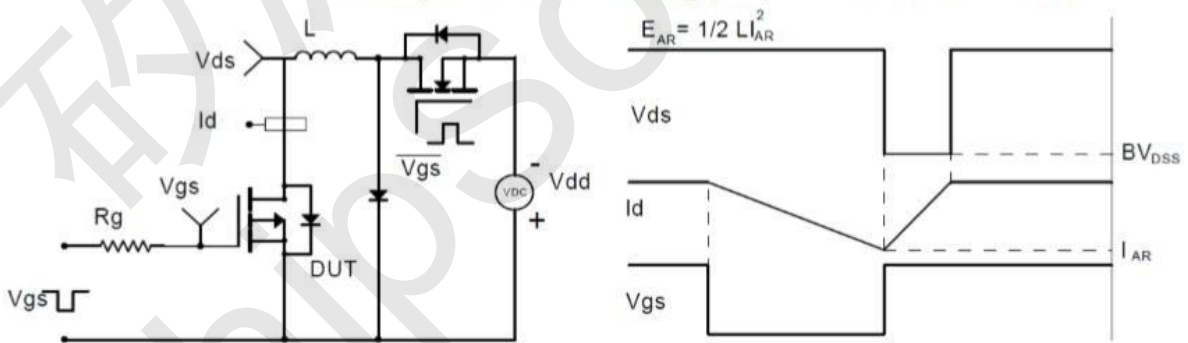
Gate Charge Test Circuit & Waveform



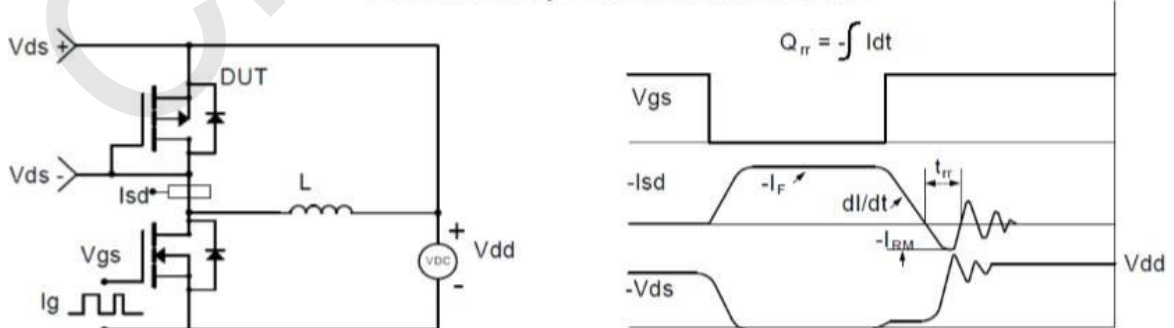
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

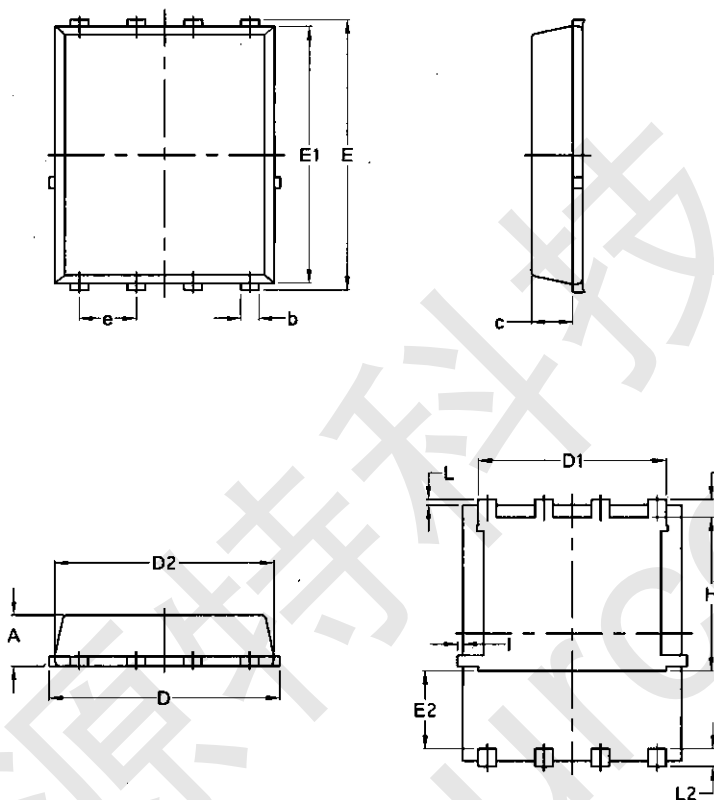


Diode Recovery Test Circuit & Waveforms





CST60P04F Package Mechanical Data-PDFN5060-8L Single



Symbol	Common		Inch	
	mm			
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070